HIGH SPEED COMPARATOR WITH BLOCKING SWITCHES FOR SAR CONVERTOR

ABSTRACT OF THE DISCLOSURE

Open loop common mode driver for switched capacitor input to SAR. A method for controlling the operation of a SAR conversion cycle. The method includes the steps of first initiating the SAR conversion cycle by connecting one side of a plurality of capacitors in a capacitor array to a first capacitor reference voltage and the other side of the plurality of capacitors to the input of a comparator. This is followed by the step of sequentially switching in a plurality of compare cycles the one side of a select one or ones of the capacitors to a second capacitor reference voltage to change the voltage on the input of the comparator. Then, a compare operation is initiated after initiation of each compare cycle to compare the value on the input of the comparator with a compare reference voltage after a predetermined settling time has elapsed from the beginning of the initiation of each compare cycle. During the compare cycle, transients due to voltage variations on the input of the comparator are reduced as a result of the step of sequentially switching, the reduction operating for a predetermined portion of the associated compare cycle.